REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-14 are in this case. Claims 1-4, 6 and 8-11 have been rejected under § 102(b). Claims 1-3, 5, 7 and 12-14 have been rejected under § 102(e).

The claims before the Examiner are directed toward an electronic module that includes electronic circuitry and first and second connection mechanisms, both operationally connected to the electronic circuitry, for mounting the module on a larger electronic device by different respective methods.

§ 102(b) Rejections - Hamzehdoost '415

The Examiner has rejected claims 1-4 and 6 under § 102(b) as being anticipated by Hamzehdoost, US Patent No. 5,999,415 (henceforth, "Hamzehdoost '415"). The Examiner's rejection is respectfully traversed.

Hamzehdoost '415 teaches a HBGA package **100** in which an integrated circuit die **102** is electrically connected to solder balls such as solder ball **190**. These solder balls are the *only* connection mechanism provided by Hamzehdoost '415 for mounting HBGA package on a larger electronic device. Therefore, Hamzehdoost '415 has nothing whatsoever to do with the present invention as recited in claim 1.

The Examiner has identified hole **182** of Hamzehdoost '415 as a second connection mechanism. Applicant fails to understand how a hole can function as a connection mechanism for die **102**. Applicant conjectures that the Examiner intended to identify pin **180** as a second connection mechanism. Even so, as best understood, pin **180** would be made of an insulating material and so would not serve as a second connection mechanism.

The Examiner also has identified conductive traces **132** of Hamzehdoost '415 as "electronic circuitry". In fact, conductive traces **132** are purely electrical, and are not at all electronic. Attached please find a definition of "electronics" dated July 6, 2003:

> **Electronics** is the science and technology of electronic circuits and devices such as thermionic valves and semiconductors using the physics of electricity. This knowledge is applied in devices that manipulate electric currents and electromagnetic fields for the controlling or processing of information, or the conversion and distribution of electrical power. (emphasis added)

So a minimal requirement for electrically conducting circuitry to be "electronic circuitry" and not merely "electrical circuitry" is that the circuitry does not merely passively conduct electrical current, but also manipulates the electrical current. Conductive traces **132**, that passively conduct electrical current between wire-bonding sites **128** and contact areas **130**, are clearly not electronic. The only electronic circuitry in HBGA package **100** is the integrated circuit on integrated circuit die **102**.

With independent claim 1 allowable as filed, it follows that claims 1-4 and 6, that depend therefrom, also are allowable.

§ 102(b) Rejections – Sawai et al. '883

The Examiner has rejected claims 1, 2 and 8-11 under § 102(b) as being anticipated by Sawai et al., US Patent No. 5,814,883 (henceforth, "Sawai et al. '883"). The Examiner's rejection is respectfully traversed.

Sawai et al. '883 teach a package for a semiconductor chip **9** in which chip **9** is electrically connected to external electrodes **14** via wires **10**, fingers **3** and copper films ***4b*** of through-holes **4**. External electrodes **14** are the *only* connection mechanism provided by Sawai et al. '883 for mounting the package on a larger

electronic device. Therefore, Sawai et al. '883 has nothing whatsoever to do with the present invention as recited in claim 1.

The Examiner has identified fingers **3** of Sawai et al. '883 as "electronic circuitry". In fact, fingers **3**, like conductive traces **132** of Hamzehdoost '415, are purely electrical, and are not at all electronic. Fingers **3** passively conduct electrical current between wires **10** and copper films **4*b***. The only electronic circuitry in the package of Sawai et al. '883 is the electronic circuitry on semiconductor chip **9**.

The Examiner also has identified "pads, shown along the bottom but not specifically referenced" as a second connection mechanism. Applicant understands the Examiner to be interpreting the flared bottoms of copper films **4*b***, as illustrated in Figure 6, as pads that can be used to mount the package of Sawai et al. '883 on a larger electronic device. It is true that the flared bottoms of copper films **4*b*** emerge from the package of Sawai et al. '883 and are electrically connected to semiconductor chip **9** via fingers **3** and wires **10**. Nevertheless, it is improper for the Examiner to interpret the teachings of Sawai et al. '883 as anticipating claim 1. Sawai et al. '883 neither state nor hint nor suggest that the flared bottoms of copper films **4*b*** can be used to provide electrical connections to semiconductor chip **9**. It is only with impermissible hindsight that the flared bottoms of copper films **4*b*** can be interpreted as a second connection mechanism.

With independent claim 1 allowable as filed, it follows that claims 2 and 8-11, that depend therefrom, also are allowable.

§ 102(e) Rejections – Hashimoto '718

The Examiner has rejected claims 1-3, 5, 7 and 12-14 under § 102(e) as being anticipated by Hashimoto, US Patent No. 6,483,718 (henceforth, "Hashimoto '718"). The Examiner's rejection is respectfully traversed.

Hashimoto '718 teaches a semiconductor device that consists of a stack of semiconductor chips **10** mounted on (presumably electrically insulating) substrates **20**. More specifically, each semiconductor chip is mounted on a (presumably electrically conducting) interconnecting pattern **30** on one surface of a respective substrate **20**. The upper interconnecting patterns **30** are electrically connected to the lowest interconnecting pattern **30** via first terminals **40**. Second terminals **50** emerge from the lowest substrate **20** to provide electrical connection between the lowest interconnecting pattern **30** and "other elements" (column 8 line 59). Second terminals **50** are the *only* connection mechanism provided by Hashimoto '718. Therefore, Hashimoto '718 has nothing to do with the present invention as recited in claim 1.

The Examiner, in identifying electrical connections **32** and first terminals **41** as "connection mechanisms", has implicitly identified interconnecting pattern **30** of the lowest substrate **20** as "electronic circuitry". In fact, interconnecting patterns **30** of Hashimoto '718, like conductive traces **132** of Hamzehdoost '415 and fingers **3** of Sawai et al. '883, are purely electrical, and are not at all electronic. Interconnecting patterns **30** passively conduct electricity between bumps **14** of semiconductor chips **10** and terminals **40** or **50**. The *only* electronic circuitry in Hashimoto '718 is on semiconductor chips **10**, each one of which is provided with a *single* connection mechanism: electrodes **12** and bumps **14**.

With independent claim 1 allowable as filed, it follows that claims 2, 3, 5, 7 and 12-14, that depend therefrom, also are allowable.

In view of the above remarks it is respectfully submitted that independent claim 1, and hence dependent claims 2- 14 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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